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TITLE

METHOD OF FORMING A MEMORY CELL WITH A SINGLE SIDED BURIED STRAP

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to a method of fabricating a memory cell with a transistor, and more particularly, to a method of forming a dynamic random access memory (DRAM) cell having a single sided buried strap.

Description of the Related Art

10 A DRAM cell comprises a metal-oxide-semiconductor field effect transistor (MOSFET) and a capacitor formed in a semiconductor silicon substrate. There is an electrical contact between the drain of a MOSFET and the bottom storage electrodes of the adjacent capacitor, which forms a memory cell of the DRAM
15 device. A large number of memory cells make up the cell arrays which combine with the peripheral circuit to produce DRAMs.

 In recent years, MOSFET size has been continuously reduced so that the packing density of DRAM devices has increased considerably. For example, new techniques for manufacturing
20 extremely small transistor elements have been developed for 1 Giga bit DRAMs and beyond. One of the methods of increasing integration is to form a three-dimensional transistor structure, instead of the commonly used planar-type transistor.

 Figs. 1A through 1H are schematic sectional views showing
25 a partially fabricated integrated circuit structure at successive stages in forming a transistor of a DRAM cell of the prior art.

In Fig. 1A, a patterned pad layer 110 is formed on a silicon substrate 100. The pad layer 110 can comprise an oxide pad layer (not shown) and a pad nitride layer (not shown). Using the pad layer 110 as a mask, a deep trench 112 is then defined in the substrate 100 by photolithography and etching. A trench capacitor (not shown) is formed in the lower portion of the deep trench 112 by a conventional process.

In Fig. 1B, a collar oxide layer 114 is formed on the sidewall of the upper portion of the deep trench 112. The collar oxide layer 114 is located above the trench capacitor (not shown). A polysilicon layer 116 is then formed filling the deep trench 112.

In Fig. 1C, the polysilicon layer 116 is etched back until the surface of a remaining polysilicon layer 116' is lower than the surface of the substrate 100.

In Fig. 1D, by performing an etch-back process, the collar oxide layer 114 over the top surface of the remaining polysilicon layer 116' is over-etched until the top surface of a remaining collar oxide layer 114' is lower than that of the remaining polysilicon layer 116'. Thus, an opening 118 is formed.

In Fig. 1E, a doped polysilicon layer (e.g. a P or As doped polysilicon layer, not shown) is deposited on the pad layer 110 and fills the opening 118. Then, the doped polysilicon layer (not shown) is etched back to form a buried strap 120 at the bottom of the opening 118.

In Fig. 1F, an insulating layer (not shown) is formed to fill the opening 118. Then, the insulating layer (not shown) is partially etched back to form an insulating layer 122 on the buried strap 120.

In Fig. 1G, a gate oxide layer 124 is formed on the sidewall of the opening 118 by thermal oxidation. A gate 126 is then formed on the insulating layer 122.

5 In Fig. 1H, an insulating spacer 128 is formed on the sidewall of the upper portion of the opening 118. The opening 118 is then filled with conductive material to form a conductive layer 130. Next, a shallow trench isolation (STI) 132 is formed in the substrate 100 to define active areas. The pad layer 110 is then removed by CMP (chemical mechanical polishing) to obtain
10 a smooth substrate 100 surface.

In Fig. 1H, a word line 134 is formed on the conductive layer 130. A drain region 136 is formed by using the word line 134 as a mask and implanting impurities into the substrate 100. Due to the high temperature during the mentioned manufacturing
15 processes, impurities contained in the buried strap 120 out-diffuse into the substrate 100 to form a source region 138, as show in Figs. 1G and 1H.

With reference to Fig. 1H, the source region 138 formed by the conventional method is circular, and the distance "d"
20 between adjacent source regions 138, and 138 is shortened when DRAM cells are scaled down. The gap created between adjacent source regions causes a serious leakage problem (also referred to as a buried strap mergence issue), reducing device reliability.

25 In U.S. Patent No. 6,432,774, Heo et al disclose a method of fabricating a DRAM cell having a vertical transistor. Though this method can form a memory cell with a single sided source region, the source region of the memory cell nevertheless faces an adjacent memory cell. Thus, the leakage problem occurs when
30 the design rule is below 0.11 μ m.

In U.S. Patent No. 5,519,236, Ozaki discloses a DRAM cell having a vertical transistor. The method removes an oxide layer on one side by photolithography using a photoresist layer as a mask. A memory cell with a single sided source region can thus
5 be formed. Nevertheless, this method suffers from misalignment issue during photolithography, making it unsuitable suitable for use in the narrower trench process.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method
10 of forming a memory cell having a vertical transistor.

Another object of the present invention is to provide a method of forming a DRAM cell with a single sided buried strap.

In order to achieve these objects, the present invention provides a method of forming a memory cell with a single sided
15 buried strap. A substrate having a trench is provided. A trench capacitor is formed at a lower portion of the trench. A collar insulating layer is formed on a sidewall of an upper portion of the trench. A first conductive layer is formed above the trench capacitor and fills the trench. Part of the first conductive
20 layer and part of the collar insulating layer are removed to form a remaining first conductive layer and a remaining collar insulating layer in an opening, wherein the opening has a first sidewall and a second sidewall, and a top surface of the remaining collar insulating layer is lower than that of the
25 remaining first conductive layer. An angle implantation with fluorine-containing ions is performed on the first sidewall of the opening. A thermal oxidation process is performed to form a first oxide layer on the first sidewall and a second oxide layer on the second sidewall, wherein a thickness of the first oxide

layer is greater than that of the second oxide layer. The second oxide layer is removed to expose the second sidewall. A second conductive layer serving as a buried strap is formed at a bottom of the opening, wherein the second conductive layer is insulated
5 from the first sidewall by the first oxide layer.

The present invention improves on the prior art in that the angle implantation with fluorine-containing ions causes the first oxide layer on the first sidewall to be greater than the second oxide layer on the second sidewall. The second oxide
10 layer is removed to expose the second sidewall, the first oxide layer, however, remains on the first sidewall. A single sided buried strap is then formed at the bottom of the opening. Thus, the single sided buried strap is insulated from the first sidewall by the first oxide layer, thereby solving the leakage
15 problem between adjacent source regions. In addition, the present invention is well suited to the 0.11 μ m (or below) trench technology, thereby achieving the goal of reduction in IC size and ameliorating the disadvantages of the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

20 The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein:

25 Figs. 1A~1H are schematic sectional views showing a partially fabricated integrated circuit structure at successive stages in forming a transistor of a DRAM cell of the prior art; and

Figs. 2A~2J are schematic sectional views showing a partially fabricated integrated circuit structure at successive

stages in forming a transistor of a DRAM cell of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

An embodiment according to the present invention will be explained with reference to Figs. 2A~2J.

In Fig. 2A, a semiconductor substrate 200 is provided. The semiconductor substrate 200 is composed of silicon or germanium. The semiconductor substrate 200 can be made by epitaxial silicon or silicon on insulator. For simplicity, a P-type semiconductor silicon substrate 200 is given as an example in this invention. A patterned pad layer 210 composed of a pad oxide layer (such as SiO_2) 202 and a silicon nitride layer 204 (such as Si_3N_4) is formed on part of the substrate 200. The pad oxide layer 202 can be formed by oxidation and the silicon nitride layer 204 can be formed by CVD (chemical vapor deposition). The thickness of the pad layer 210 is about 1500 to 3000Å. Using the pad layer 210 as a mask, part of the substrate 200 is removed to form a deep trench 212 therein. A trench capacitor (not shown) is then formed at the lower portion of the deep trench 212 by conventional processes, as disclosed in U.S. Patent Nos. 6,190,988, 6,326,261, and the others. In order to avoid obscuring the aspects of the present invention, the trench capacitor process is not described here.

In Fig. 2B, a collar insulating layer 214 is formed on the sidewall of an upper portion of the deep trench 212 above the trench capacitor (not shown). The collar insulating layer 214 can be a silicon oxide (SiO_2) layer formed by CVD. The thickness of the collar insulating layer 214 is about 200 to 1000Å. A first conductive layer 216 is formed above the trench capacitor (not

shown). The first conductive layer 216 fills the inner space of the deep trench 212 and expands on the pad layer 210. The first conductive layer 216 is usually composed of polysilicon doped with arsenic ions or phosphorus ions formed by CVD.

5 In Fig. 2C, using the pad layer 210 as a stop layer, the first conductive layer 216 above the pad layer 210 is removed by performing a planarization process, such as CMP (chemical mechanical polishing). An etch-back process is then performed to remove a portion of the first conductive layer 216 to a first
10 determined depth, and thus a remaining first conductive layer 216' is formed. That is, the top surface of the remaining first conductive layer 216' is lower than the surface of the substrate 200. The first determined depth is about 3000~5000Å beneath the surface of the substrate 200.

15 In Fig. 2D, a portion of the collar insulating layer 214 is removed to form a remaining collar insulating layer 214' in an opening 218 by over-etching process until the top surface of the remaining collar insulating layer 214' is lower than that of the remaining first conductive layer 216'. The opening 218
20 has a first sidewall 2181 and a second sidewall 2182.

 Fig. 2E shows the key step of the present invention. An angle implantation 220 with fluorine-containing ions is performed on the first sidewall 2181 of the opening 218. The fluorine-containing ions can comprise F and/or BF₂ ions. An
25 operating condition of the implantation 220 is provided, but is not intended to limit the present invention. For example, the implantation energy is 15~30keV and the ion dosage is 1E14~4.5E15 ions/cm².

 In Fig. 2F, a thermal oxidation process of 900~950°C is
30 performed to form a first oxide layer 224 on the first sidewall

2181 and a second oxide layer 226 on the second sidewall 2182, wherein a thickness "b" of the first oxide layer 224 is greater than a thickness "c" of the second oxide layer 226. The oxide layers 224 and 226 can be SiO₂ layers. It is noted that the first oxide layer 224 with thickness "b" is preferably greater than the remaining collar insulating layer 214' with thickness "a". The mechanism and experimental results of the oxide thickness of the F/BF₂-implanted layer being two or three times that of the un-implanted layer in a thermal oxidation process at 900~950°C, which are disclosed by Debra S. Woolsey and in the article entitled "Enhanced discrete DMOS power trench gate oxide growth" in the Journal of Solid State Technology No. 31, October 2002.

In Fig. 2G, using isotropic etching (e.g. wet etching) with time mode, the second oxide layer 226 is removed to expose the second sidewall 2182 of the opening 218. At this time, the first oxide layer 224 remains on the first sidewall 2181. It is noted that, due to the first oxide layer 224 being greater than the second oxide layer 226, a mask to protect the first oxide layer 224 during this etching step is not required.

In Fig. 2G, by performing deposition and etch-back processes, a second conductive layer 228 serving as a buried strap 228 is formed at the bottom of the opening 218, wherein the second conductive layer 228 is insulated from the first sidewall 2181 by the first oxide layer 224. The second conductive layer 228 is composed of polysilicon doped with impurities, such as arsenic ions or phosphorus ions.

In Fig. 2H, an insulating layer 230 is formed on the second conductive layer 228. The insulating layer 230 can be a SiO₂ layer formed by CVD. The insulating layer 230 is commonly called

a trench top oxide (TTO) layer. A gate insulating layer 232 is then formed on the second sidewall 2182 by thermal oxidation at 800~1000°C. The gate insulating layer 232 can be a SiO₂ layer.

In Fig. 2H, a third conductive layer 234 serving as a gate 5 234 is formed in part of the opening 218. The third conductive layer 234 can be composed of polysilicon doped with arsenic ions or phosphorus ions. Due to the high temperature during the mentioned and subsequent manufacturing processes, the impurities contained in the buried strap 228 (i.e. the second 10 conductive layer) out-diffuse into the substrate 200 to form a source region 236, as show in Figs. 2H~2J.

In Fig. 2I, by performing deposition and etch-back processes, an insulating spacer 238 is formed on the sidewall of the upper portion of the opening 218. The insulating spacer 15 238 can be a SiO₂ layer. Next, a fourth conductive layer 240 fills the opening 218. The pad layer 210 is removed by a planarization process such as CMP, thus a smooth substrate 200 surface is obtained. A shallow trench isolation (STI) 242 is then formed in the substrate 200 to define active areas.

20 In Fig. 2J, a fifth conductive layer 244 serving as a word line 244 is formed on the fourth conductive layer 240. A drain region 246 is then formed by using the word line 244 as a mask and implanting impurities (e.g. arsenic ions or phosphorus ions) into the substrate 200.

25 The present invention uses the angle implantation with fluorine-containing ions and the oxidation process of 900~950°C to form the thick first oxide layer on the first sidewall and the thin second oxide layer on the second sidewall. The second oxide layer is removed to expose the second sidewall, the first 30 oxide layer, however, remains on the first sidewall. A single

sided buried strap is then formed at the bottom of the opening. Thus, the single sided buried strap is insulated from the first sidewall by the first oxide layer, thereby preventing leakage between adjacent source regions. In addition, the present
5 invention is well suited to the 0.11 μ m (or below) trench technology, thereby achieving the goal of reduced IC size and ameliorating the disadvantages of the prior art.

Finally, while the invention has been described by way of example and in terms of the above, it is to be understood that
10 the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such
15 modifications and similar arrangements.